CLAIMS

Sub B3

1. A semiconductor integrated circuit connected to an external processor comprising:

a memory which stores data;

a terminal which connects the memory with the processor;

an information generation circuit which generates production information about the semiconductor integrated circuit; and

a write circuit which writes the information into the memory before the semiconductor integrated circuit starts normal operation.

2. The semiconductor integrated circuit according to claim 1,

wherein the write circuit writes the information into the memory after the semiconductor integrated circuit is reset.

3. The semiconductor integrated circuit according to claim 1 ~~or 2~~,

wherein the write circuit writes the information into the memory when a command from the processor ends.

4. The semiconductor integrated circuit according to ~~any one of claims 1 to 3~~ claim 1,

wherein the write circuit writes the information into the memory when a sleep state of the semiconductor integrated

circuit is released.

5. The semiconductor integrated circuit according to ~~any one of claims 1 to 4~~ CLAIM 1,

wherein the memory is a cache memory being accessed by the processor.

6. The semiconductor integrated circuit according to ~~any one of claims 1 to 5~~ CLAIM 1, further comprising:

a register which receives address data of the area where the information is written, from the processor, and stores the address data into the memory.

7. The semiconductor integrated circuit according to ~~any one of claims 1 to 6~~ CLAIM 1,

wherein the information comprises at least one of a production history and a manufacturer's name of the semiconductor integrated circuit.

8. A semiconductor integrated circuit connected to a combination of an external memory and a processor comprising:

a terminal connected to the external memory;

an information generation circuit which generates production information about the semiconductor integrated circuit; and

a write circuit which writes the information into the external memory through the terminal before the semiconductor

integrated circuit starts normal operation.

9. The semiconductor integrated circuit according to claim 8,

wherein the write circuit writes the information into the external memory after the semiconductor integrated circuit is reset.

10. The semiconductor integrated circuit according to claim 8 ~~or 9~~,

wherein the write circuit writes the information into the external memory when a command from the processor ends.

11. The semiconductor integrated circuit according to ~~any one of claims 8 to 10~~ claim 8,

wherein the write circuit writes the information into the external memory when a sleep state of the semiconductor integrated circuit is released.

12. The semiconductor integrated circuit according to ~~any one of claims 8 to 11~~ claim 8, further comprising:

a register which receives address data of the area where the information is written, from the processor, and stores the address data into the external memory.

13. The semiconductor integrated circuit according to ~~any one of claims 8 to 12~~ claim 8,

wherein the information comprises at least one of a production history and a manufacturer's name of the semiconductor integrated circuit.

14. A semiconductor integrated circuit having a built-in processor comprising:

a memory which is connected to the processor and stores data;

an information generation circuit which generates production information about the semiconductor integrated circuit; and

a write circuit which writes the information into the external memory through the terminal before the semiconductor integrated circuit starts normal operation.

15. The semiconductor integrated circuit according to claim 14,

wherein the write circuit writes the information into the memory after the semiconductor integrated circuit is reset.

16. The semiconductor integrated circuit according to claim 14 ~~or 15~~,

wherein the write circuit writes the information into the memory when a command from the processor ends.

17. The semiconductor integrated circuit according to ~~any one of claims 14 to 16~~ claim 14,

wherein the write circuit writes the information into the memory when a sleep state of the semiconductor integrated circuit is released.

18. The semiconductor integrated circuit according to ~~any one of claims 14 to 17~~ CLAIM 14,

wherein the memory is a cache memory being accessed by the processor.

19. The semiconductor integrated circuit according to ~~any one of claims 14 to 18~~ CLAIM 14, further comprising:

a register which receives address data of the area where the information is written, from the processor, and stores the address data into the memory.

20. The semiconductor integrated circuit according to ~~any one of claims 14 to 19~~ CLAIM 14,

wherein the information comprises at least one of a production history and a manufacturer's name of the semiconductor integrated circuit.